MPW GDS Submission Package

Project Information	
Project Name:	[PROJECT_NAME]
Tapeout Date:	[TAPEOUT_DATE]
Submission Deadline:	[DEADLINE]
MPW Provider:	[PROVIDER_NAME]
Process Node:	[PROCESS_NODE]

Package Contents

This submission package contains the following directory structure:

```
├── 01_GDS_Files/
│   ├── [CHIP_NAME].gds        # Main GDS file (DRC/LVS Clean)
│   ├── [CHIP_NAME].oasis      # Optional OASIS format if required
│   └── cell_library/          # Any custom cell libraries not in PDK
│
├── 02_Documentation/
│   ├── Design_Intent.pdf      # Overall chip description and function
│   ├── Pin_List.csv           # Complete list of pins with function
│   ├── Block_Diagram.pdf      # High-level block diagram
│   └── Special_Requirements.pdf # Any special process/handling needs
│
├── 03_Verification_Reports/
│   ├── drc_report/            # Final Design Rule Check reports
│   ├── lvs_report/            # Final Layout vs. Schematic reports
│   ├── antenna_report/        # Final Antenna rule check reports
│   └── density_report/        # Final Metal density reports
│
├── 04_Bonding_Packaging/
│   ├── [CHIP_NAME]_bonding_diagram.pdf # Bonding diagram (matches GDS)
│   ├── [CHIP_NAME]_pad_coordinates.csv # Pad coordinates table
│   └── Package_Requirements.pdf        # Package specifications
│
├── 05_Test_Requirements/
│   ├── Test_Guide.pdf         # Guide for testing the chip
│   └── Known_Issues.pdf       # Any known issues or limitations
│
└── README.md                  # This file
```

Submission Checklist

- [x] GDS file(s) have been verified with final DRC run
- [x] GDS file(s) have correct units and database precision
- [x] All verification reports are clean or have documented waivers
- [x] Bonding diagram matches pad ring in GDS
- [x] All required forms have been completed
- [x] Design meets area and aspect ratio requirements
- [x] Final LVS reports show clean comparison
- [x] Metal density requirements are met for all layers
- [x] Seal ring/scribe line implementation is correct
- [x] All custom IP has correct licensing documentation

GDS File Information

Parameter	Value
Main GDS File:	[CHIP_NAME].gds
File Size:	[SIZE] MB
Top Cell Name:	[TOP_CELL_NAME]
Creation Date:	[CREATION_DATE]
Created With:	[EDA_TOOL_NAME_VERSION]
Database Unit:	[DATABASE_UNIT] meters
Layer Map File:	[LAYER_MAP_FILE].map

Required Submission Materials

Forms

- [ ] MPW Application Form
- [ ] Design Information Form
- [ ] Process Options Form
- [ ] IP Declaration Form
- [ ] GDS Release Form

Documentation

- [ ] Design Abstract (1-2 page summary)
- [ ] Bonding Diagram
- [ ] Layout Screenshot (Top level)
- [ ] Block Diagram

- [ ] DRC/LVS Reports (Final, clean)
- [ ] Pin List
- [ ] Process Option Selections

Design Details

Parameter	Value
Design Type:	[DIGITAL/ANALOG/MIXED_SIGNAL/RF]
Process Node:	[PROCESS_NODE]
Process Options:	[LIST_OPTIONS]
Die Size:	[WIDTH] × [HEIGHT] mm
Pad Count:	[PAD_COUNT]
Core Supply Voltage:	[CORE_VOLTAGE] V
I/O Supply Voltage:	[IO_VOLTAGE] V
Clock Frequency:	[FREQUENCY] MHz
Design IP:	[LIST_MAJOR_IP_BLOCKS]

Verification Status

DRC Status

- [x] Full Chip DRC Clean
- [ ] Waivers Required: [List specific rules waived with justification, or N/A]

LVS Status

- [x] Full Chip LVS Clean
- [ ] Floating Nets: [NO]
- [ ] Disconnected Pins: [NO]

Power Analysis Status

- [x] IR Drop Analysis Completed
- [ ] Maximum IR Drop: [IR_DROP_VALUE] mV (Target: <5% of VDD)
- [x] Electromigration Check Completed
- [ ] Worst EM Ratio: [EM_RATIO] (Target: <1.0)

Contact Information

Primary Contact

Field	Value
Name:	[PRIMARY_CONTACT_NAME]
Email:	[PRIMARY_CONTACT_EMAIL]
Phone:	[PRIMARY_CONTACT_PHONE]

Technical Contact

Field	Value
Name:	[TECHNICAL_CONTACT_NAME]
Email:	[TECHNICAL_CONTACT_EMAIL]
Phone:	[TECHNICAL_CONTACT_PHONE]

Packaging Requirements

Parameter	Value
Package Type:	[PACKAGE_TYPE]
Package Size:	[PACKAGE_SIZE]
Number of Pins:	[PIN_COUNT]
Special Requirements:	[SPECIAL_REQUIREMENTS]

Test Plan Summary

Parameter	Value
Functional Test Coverage:	[COVERAGE_PERCENTAGE]%
Main Test Equipment:	[TEST_EQUIPMENT]
Special Test Requirements:	[SPECIAL_TEST_REQUIREMENTS]

Notes & Special Instructions

[ADD_ANY_SPECIAL_INSTRUCTIONS_OR_NOTES_FOR_FOUNDRY/BROKER]